IN THE CLAIMS:

1. (currently amended): A driver circuit, having at least one input node for an input signal and at least one output node for an output signal, having one or more, preferably two, sub-drivers, and having a feedback circuit, which has one or more evaluation circuits and one or more feedback capacitors, the evaluation circuit(s) being connected to the subdriver(s) and the feedback capacitor(s) respectively being provided between an output node of the driver circuit and an input node of an evaluation circuit, the at least one evaluation circuit having a first inverter stage, coupled to the input node of the evaluation circuit, and [[also]] a second inverter stage, connected in series with the first inverter stage, the first inverter stage [being short-circuited with the input node.] comprising at least a first transistor of a first polarity and a first transistor of a second polarity, the second polarity being different from the first polarity, wherein the control terminal of the first transistor of the first polarity and the control terminal of the first transistor of the second polarity are coupled to the input node of the evaluation circuit, wherein a second terminal of the first transistor of the first polarity and a second terminal of the first transistor of the second polarity are coupled to each other and to the input node of the evaluation circuit, wherein the second inverter stage comprises at least a second transistor of the first polarity and a second transistor of the second polarity, and wherein a second terminal of the second transistor of the first polarity and a second terminal of the second transistor of the second polarity are coupled to each other and to the input node for the input signal.

2. (amended) The driver circuit as claimed in claim 1, wherein the at least one input node for the input signal is connected to the at least one sub-driver.

3. (currently amended): The driver circuit as claimed in claim 2, wherein the [at least one] input node for the input signal is connected to the [at least one] evaluation circuit.

4. (amended) The driver circuit as claimed in claim 1, wherein two or more sub-drivers and two or more evaluation circuits are provided, each sub-driver being connected to an evaluation circuit.

5. (amended) The driver circuit as claimed in claim 4, wherein two or more feedback capacitors are provided, each feedback capacitor being provided between an output node of the driver circuit and an input node of an evaluation circuit.

6. (currently amended): The driver circuit as claimed in claim 1, wherein the input node(s) of the evaluation circuit(s) is/are at low input impedance.

7 (amended) The driver circuit as claimed in claim 1, wherein the at least one sub-driver has one or more transistors.

8. (amended) The driver circuit as claimed in claim 1, wherein at least one control transistor is provided in the at least one sub-driver, said transistor being respectively connected to an evaluation circuit.

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9. (amended) The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a linear capacitor.

10. (amended) The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a nonlinear capacitor.

11. (amended) The driver circuit as claimed in claim 10, wherein the nonlinear capacitor is formed from at least one PMOS transistor and/or at least one NMOS transistor.

12. (currently amended): The [A method for operating a] driver circuit as [[claimed]] in [[one of]] claim 1 wherein a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

13. (currently amended): The driver circuit [[method]] as [[claimed]] in claim 12, wherein a $\sin^2$-shaped current is supplied to the load.

14. (currently amended): The driver circuit [[method]] as [[claimed]] in claim 12 wherein, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated therein, and wherein the driver strength of the at least one sub-driver is regulated on a [[the]] basis of the evaluation results.

15. (cancelled).

16. (currently amended): The use of a driver circuit as [[claimed]] in [[one of]] claim[[s]] 1 to improve [for improving] the electromagnetic compatibility of electronic components, in particular of integrated circuits.

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17. (new): The driver circuit as in claim 12 to improve the electromagnetic compatibility of electronic components, in particular of integrated circuits.